

# LCFC NM-D601

## Y560 M/B Schematics Document

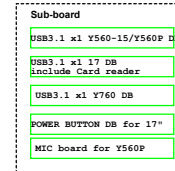
AMD-Cezanne-FP6\_BGA1140 with DDR4 + NV N20 P0/P1 GPU

2020-08-27

REV: 0.2

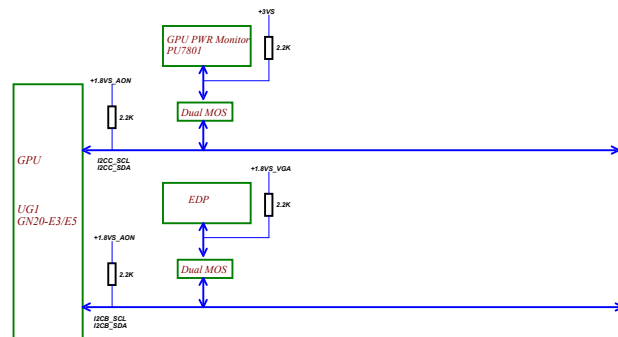
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				Y560	2.0
Date: Monday, March 29, 2021				Sheet	1 of 110

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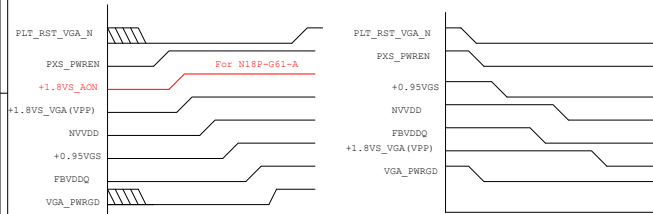


[illegible]

## GN20x-P/N18P-G61-A GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT*_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN I1V8_MAIN_EN	GN20x-P GPU power sequencing for GC6 --MSVDD_EN N18P-G61-A I1V8_MAIN_EN	GPIO4_GC6_MSVDD_EN I1V8_MAIN_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(10K PU) <b>RSVD</b>
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	iGPU_EDP_ENBKL	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRR MUX input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED			test point
GPIO24	IN	HPD_IFPF*	Hot Plug Detect for IFPF	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	test point
GPIO26	OUT	ROM_WP* FP_FUSE	GN20x-P Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)

## GN20x-P/N18P-G61-A Power Sequence



1. The ramp time for any rail must be more than 40ms and is recommended to be less than 2ms.
2. It is recommended that the delay from I1V8 on to FBVDDQ/I1V8 assertion not exceed 20ms.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVDD must be 90s before FBVDDQ can ramp-up.
5. Refer to the JESD8 Memory RPEC for memory-related power sequencing.
7. FBVDDQ, USB\_VDDP and I1V8\_AON don't need power cycle for GC6
2. All 3.3V devices that connect to the GPU must be ramp down before I1V8. GPU can NOT have any 3.3V leakage path after I1V8 power down.
3. Power down of FBVDDQ must be less than 10s before NVVDD can start ramp-down.

H-High: Tied to 1.8V  
M-Middle: Tied to 0.9V  
L-Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-P/N18P-G61-A VRAM
L	L	L	0 (0x0000)	Samsung K42803258C-HC14
L	L	H	1 (0x0001)	Micron MT61HC256M32JE-14-A
L	H	L	2 (0x0002)	Hynix Only For GN20x-P H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

## BOM Structure Control Table

BOM Structure	BTO Item
0	Not stuff
02P0	GN20-P1/P0 N18P-G61 stuff
GN200	GN20P1/P0 stuff
N18P0	N18P-G61 stuff

## FS\_OVERT# FUNCTION ENABLE

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	N18P-G61-A ENABLE OVERT*
L	L	H	GN20x-P ENABLE OVERT*

## BOM NOTE:

1.BOM Structure:  
GN20x-P1/P0-->GN200  
N18P-G61-A-->N18P0

2.1.0V GS voltage different: need Power setting  
GN20x-P1/P0-->0.95V  
N18P-G61-A-->1.0V

3.VBIOS ROM partnumber need BOM control  
GN20x-P1/P0-->2MB PN:SA00000A500  
N18P-G61-A-->1MB PN:SA000080800

4.ROM\_SO,ROM\_SI,ROM\_CLK setting  
GN20x-P1/P0-->LLH  
N18P-G61-A-->LLL

5.VRAM\_FB(RG702 STUFF package 0402)  
GN20x-P1/P0 : 2.49K ohm (PN:SD03424918J)  
N18P-G61-A: 49.9 ohm (PN:SD034499A8J)

6.+FUSE I1V8  
GN20x-P1/P0 : RG1200:10K CG1104:1U  
N18P-G61-A: RG1200:2.21K CG1104:2.2U

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	1	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1.SMB\_ALT\_ADDR ENABLE  
0.SMB\_ALT\_ADDR DISABLE  
1.DEVID\_SEL REBRAND  
0.DEVID\_SEL ORIGINAL  
1.PCIE\_CFG LOW POWER  
0.PCIE\_CFG HIGH POWER  
1.VGA\_DEVICE ENABLE  
0.VGA\_DEVICE DISABLE

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N18E VGA Notes List

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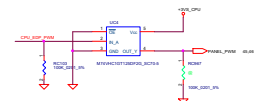
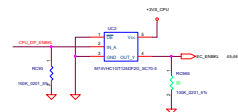
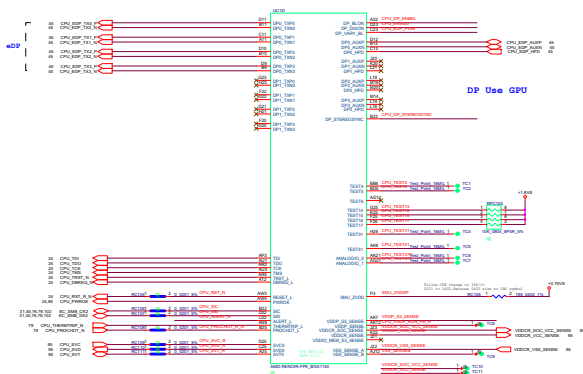
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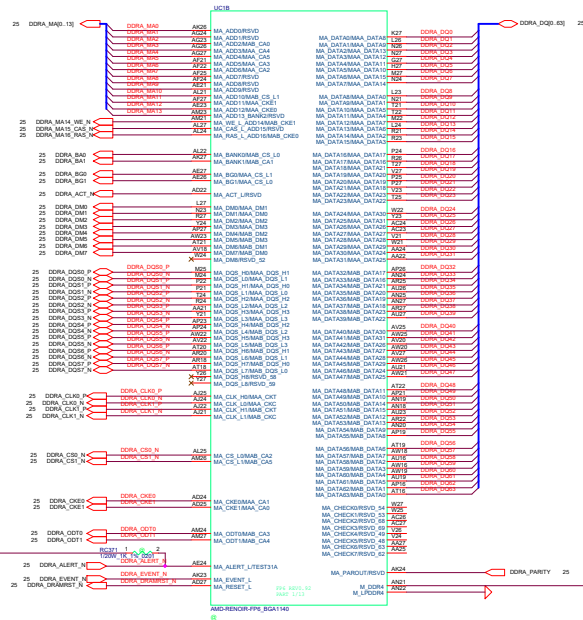
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Sheet 5 of 130

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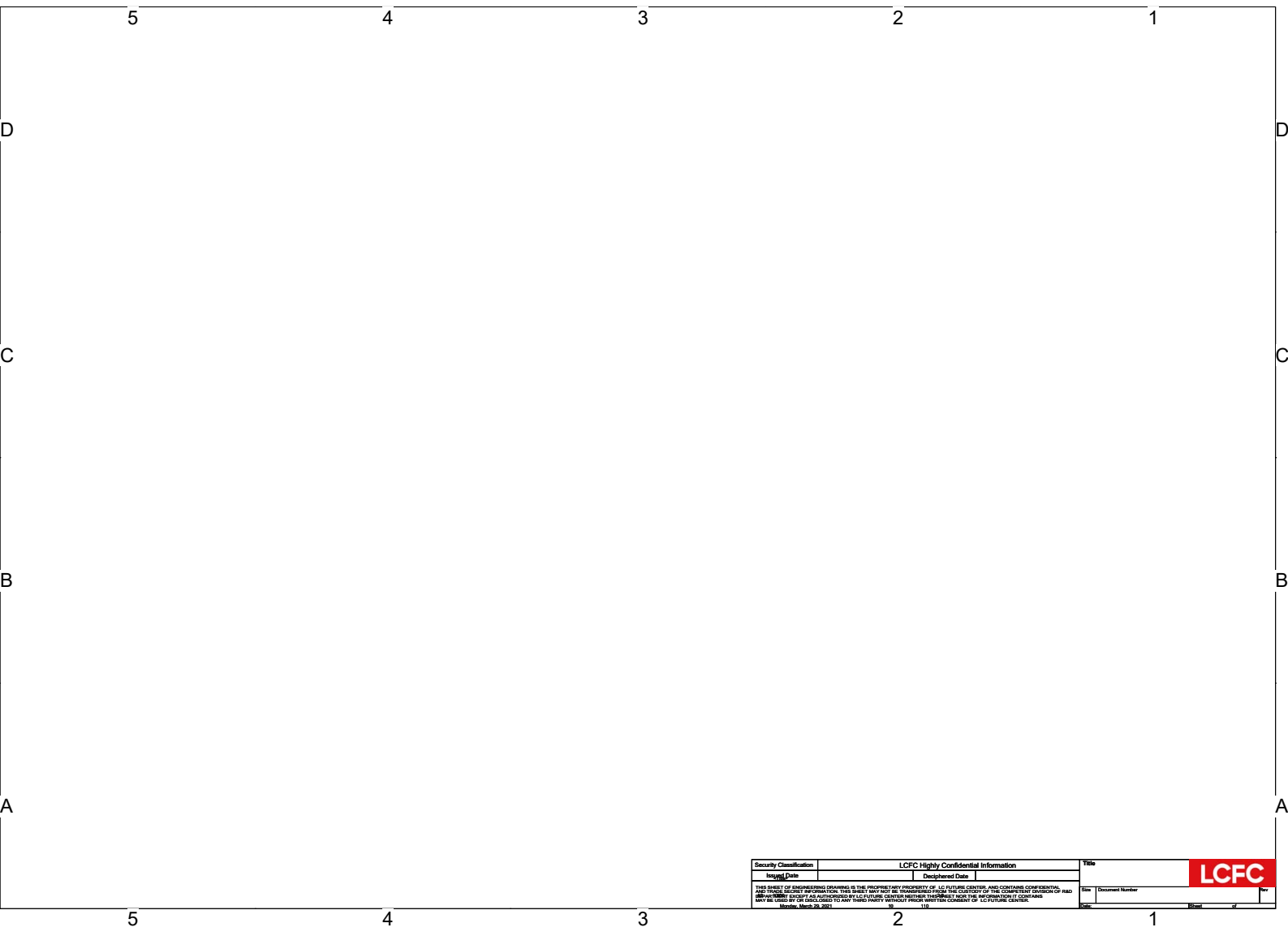




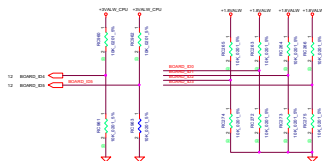
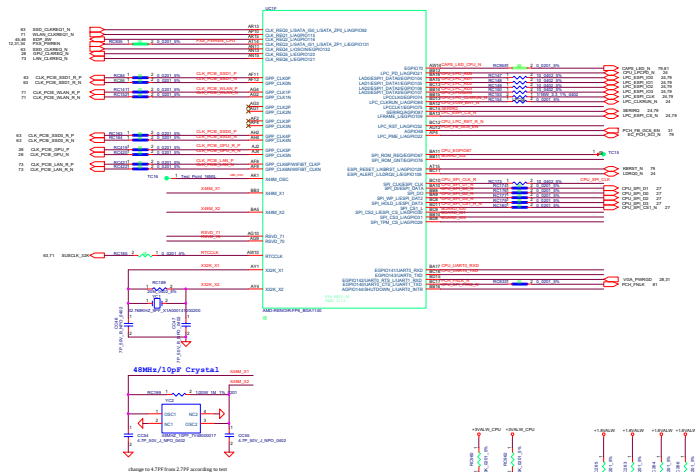
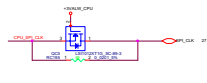




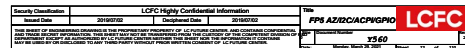




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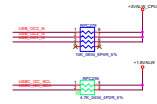
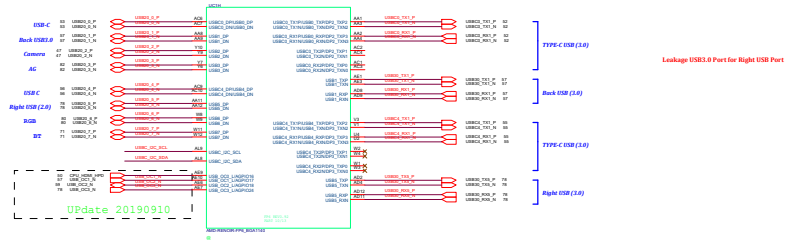
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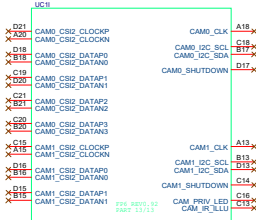
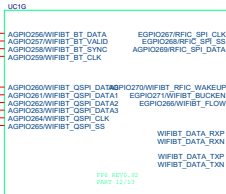
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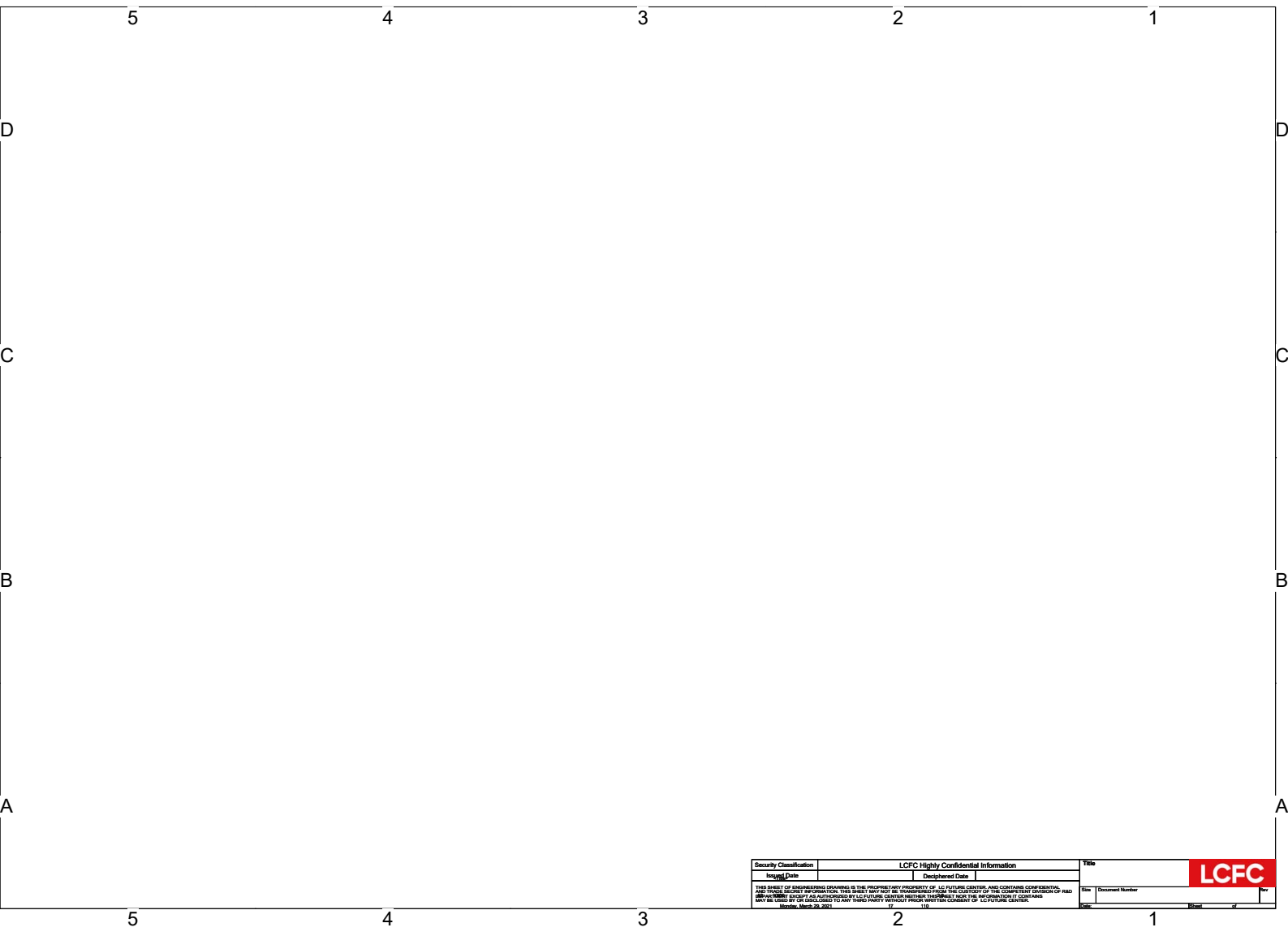




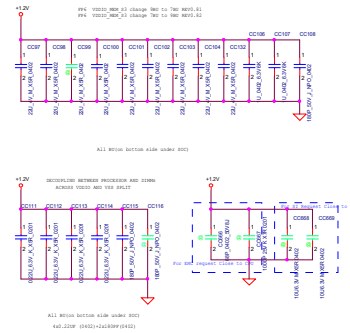
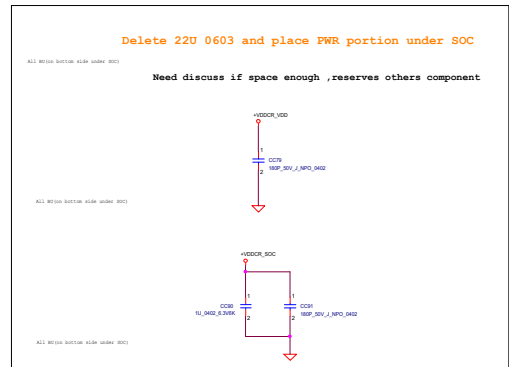
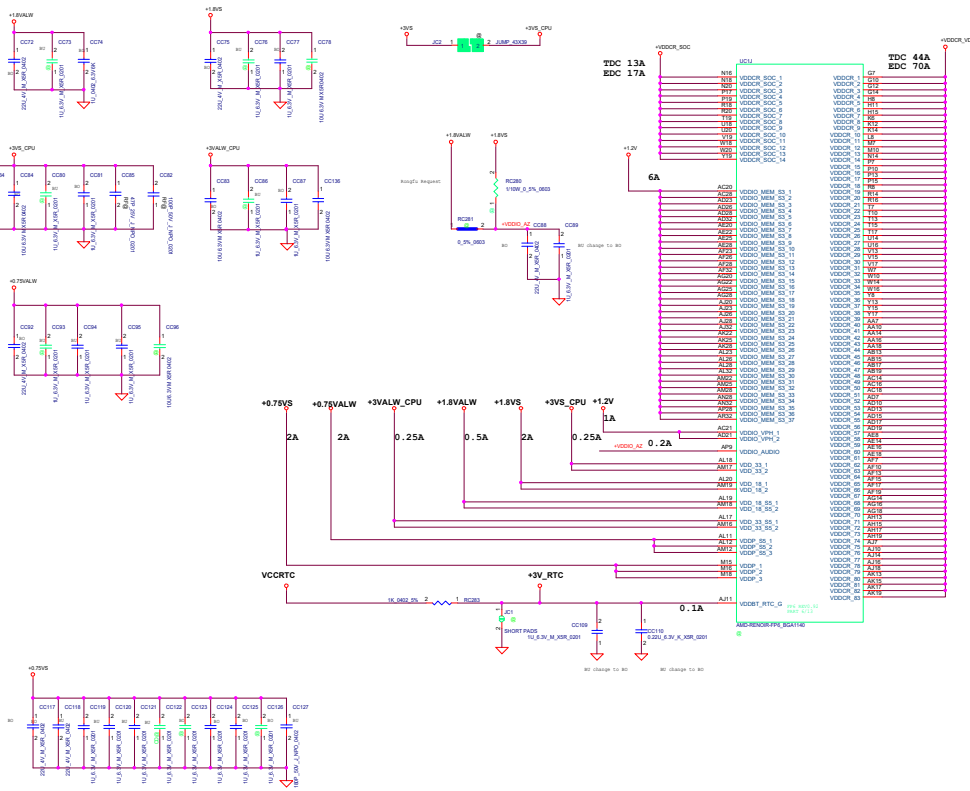
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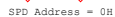








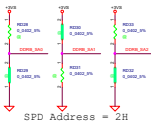
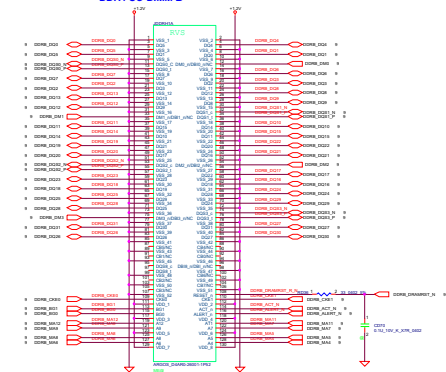




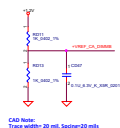
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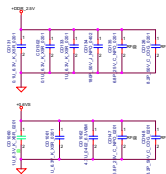
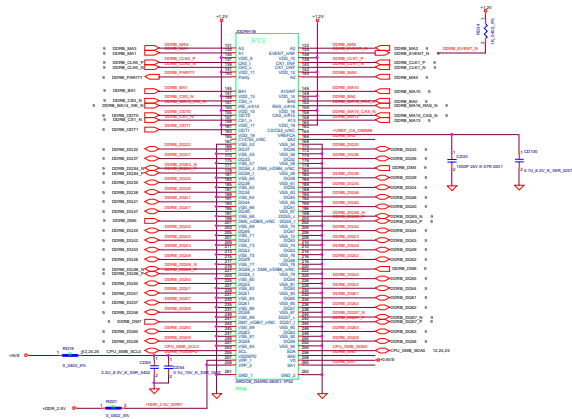
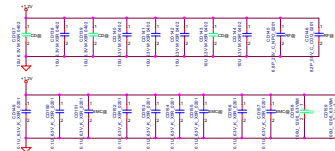
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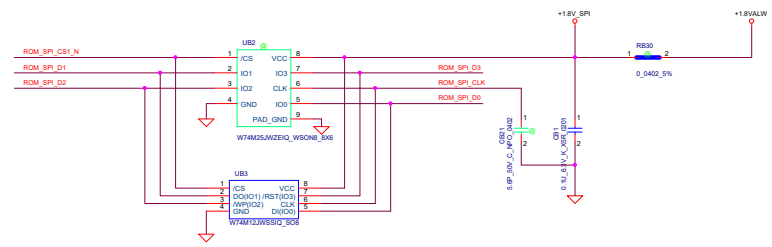
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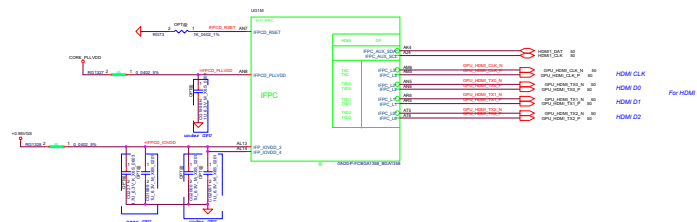
CAD Note:  
Trace width = 20 mil, Spacing = 20 mil



11	CPU_SPI_CS1_N	RB20	2	1	0.0402 5%	ROM_SPI_CS1_N
11	CPU_SPI_D0	RB21	2	1	0.0402 5%	ROM_SPI_D0
11	CPU_SPI_D1	RB22	2	1	0.0402 5%	ROM_SPI_D1
11	SPI_CLK	RB23	2	1	0.0402 5%	ROM_SPI_CLK
11	CPU_SPI_D2	RB24	2	1	0.0402 5%	ROM_SPI_D2
11	CPU_SPI_D3	RB25	2	1	0.0402 5%	ROM_SPI_D3
79	EC_SPI_CS1_N	RB13	1	2	0.0201 5%	CPU_SPI_CS1_N
79	EC_SPI_CLK	RB27	1	2	0.0201 5%	SPI_CLK
79	EC_SPI_D0	RB28	1	2	0.0201 5%	CPU_SPI_D0
79	EC_SPI_D0	RB29	1	2	0.0201 5%	CPU_SPI_D1

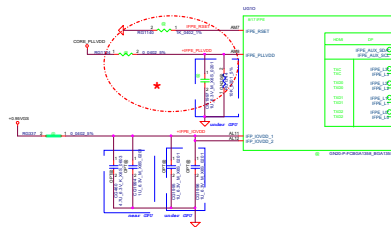


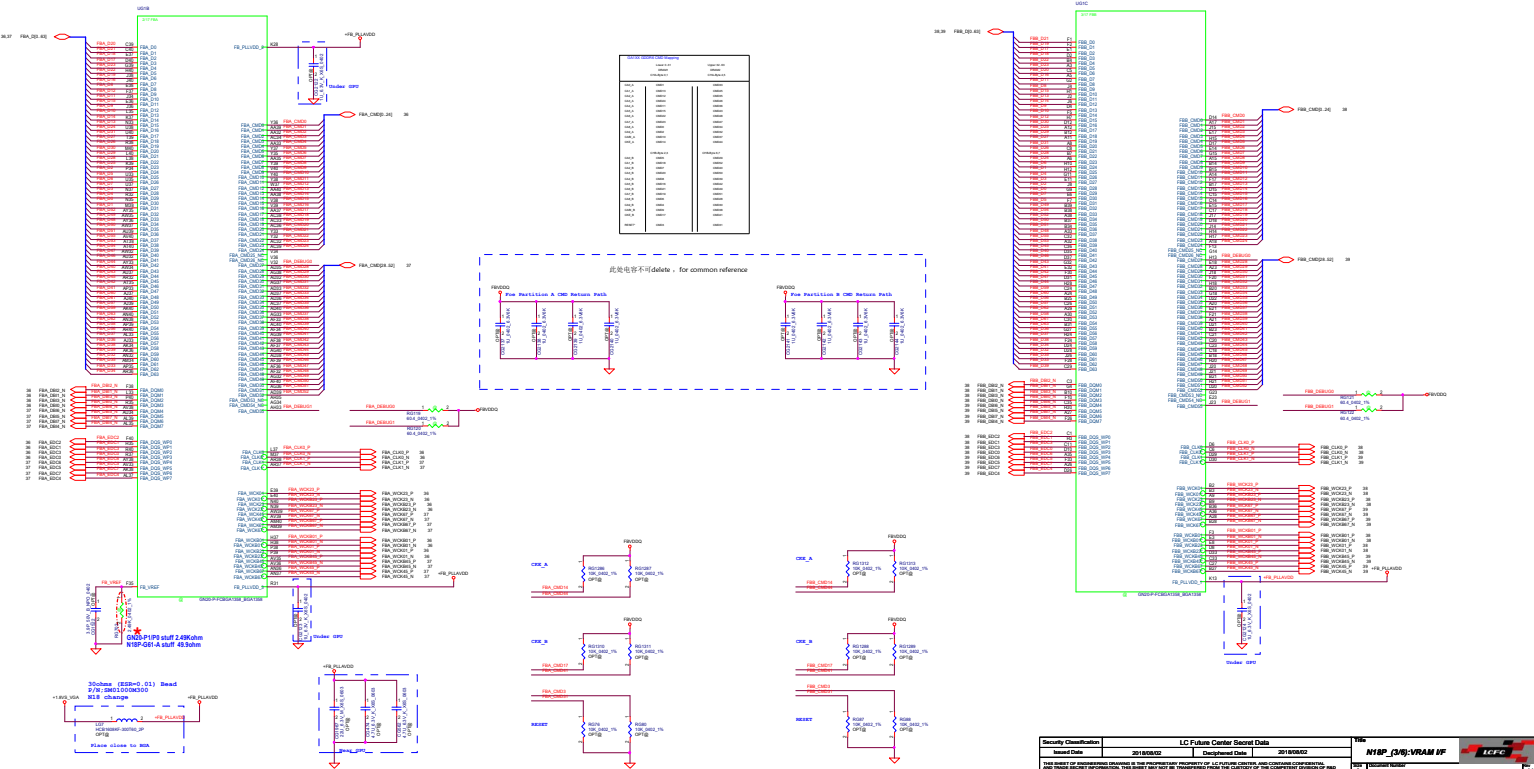


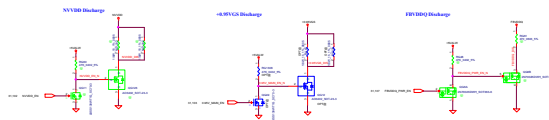
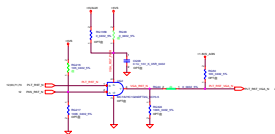


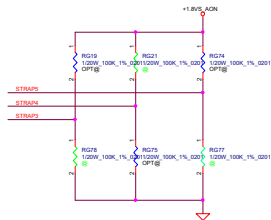
1.If an IFF link is unused, The main and AUX links, IFFxy RESET can be left unconnected, and IFFxy\_PLLVDD should be 10K PO to GND.

2.IFF\_I0VDD rail can be left unconnected if no IFF link is used. If any IFF is used, all IFF\_I0VDD balls must be connected to power rail.



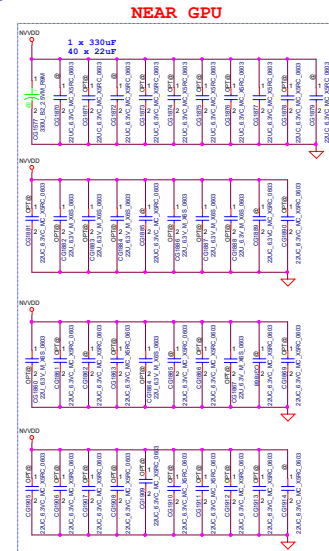
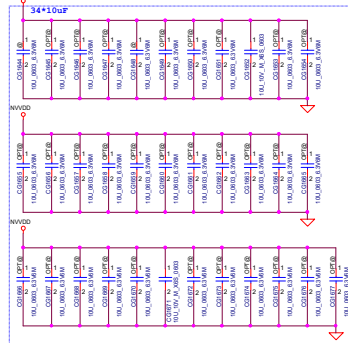
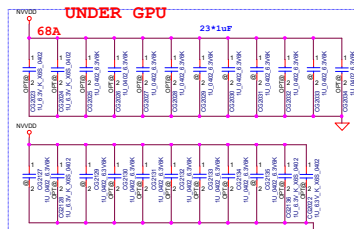
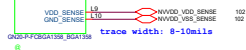
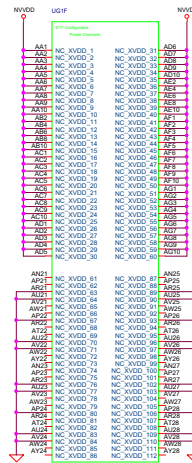
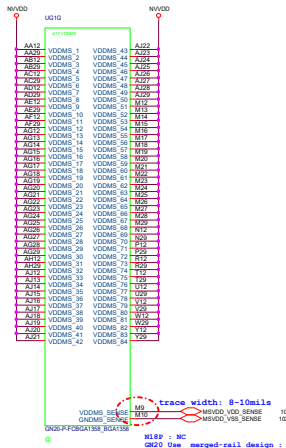
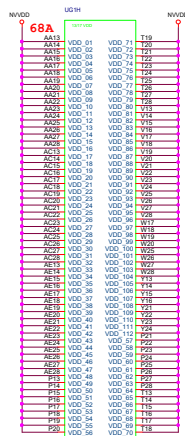


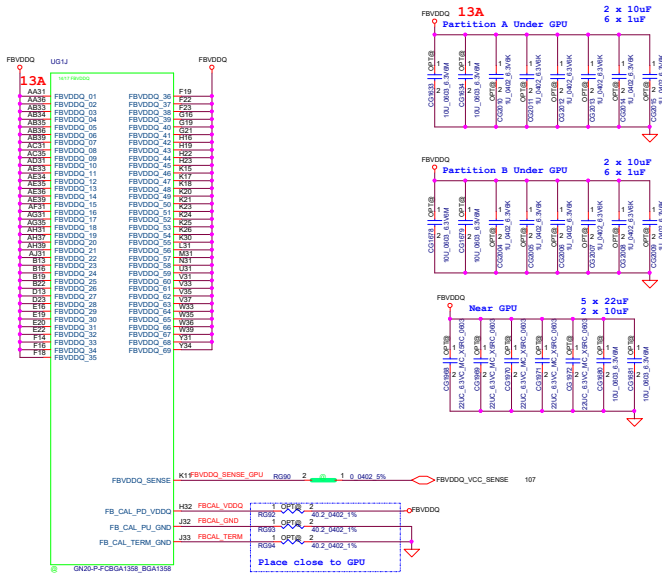




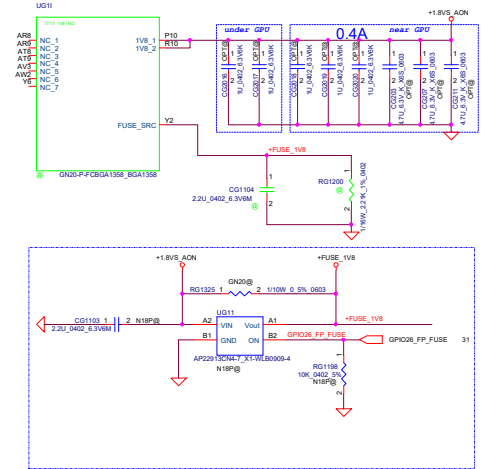
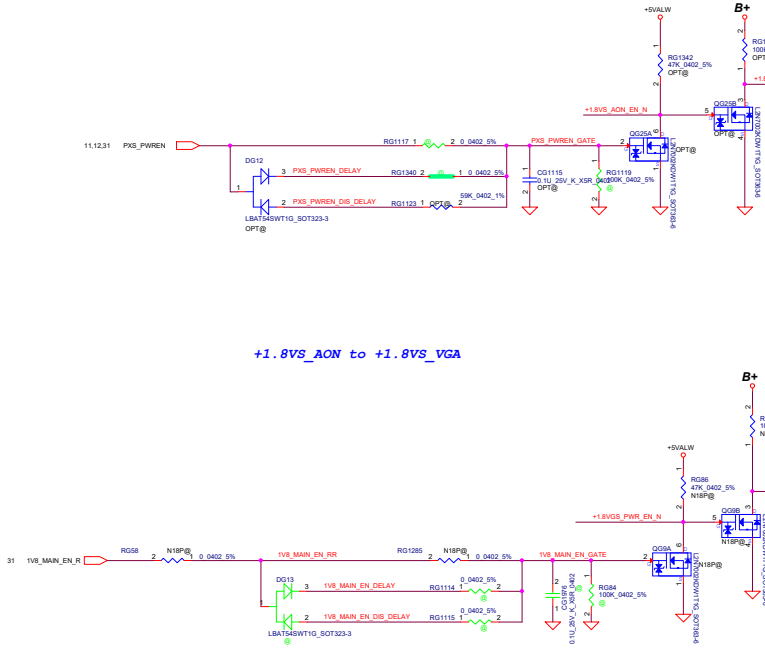
1:DEVID\_SEL for G-SYNC SKU



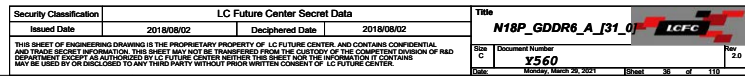


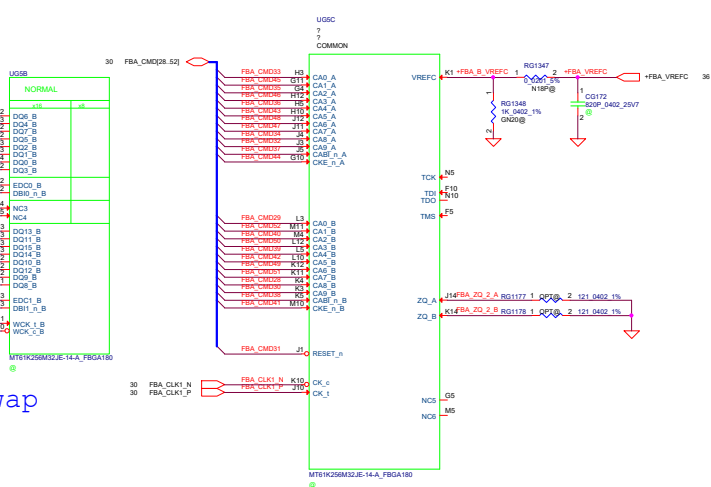


+1.8VALW to +1.8VS\_AON

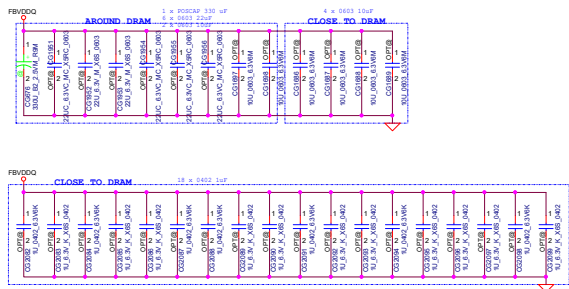
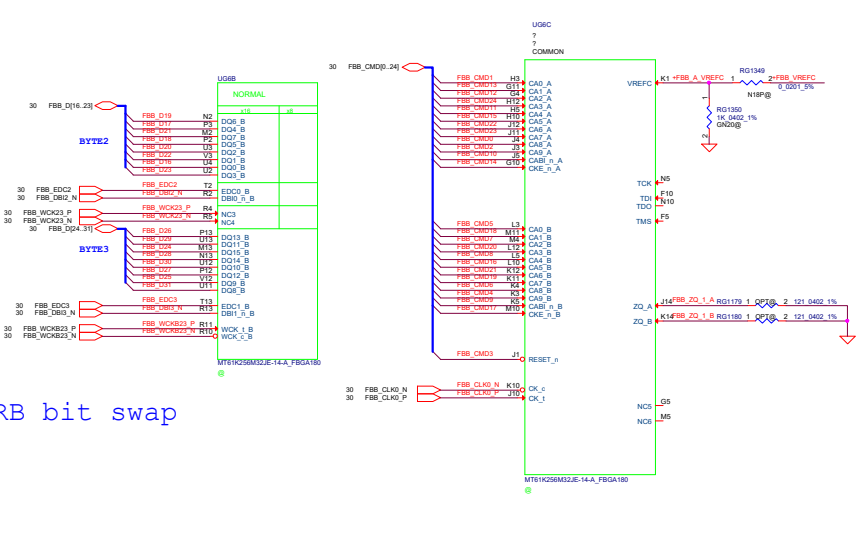
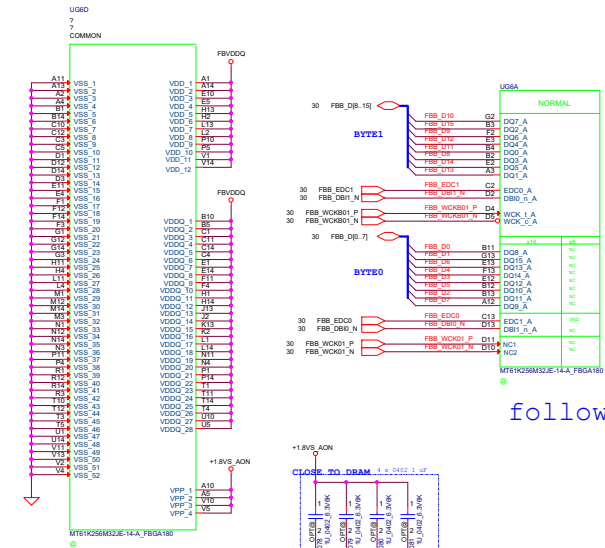




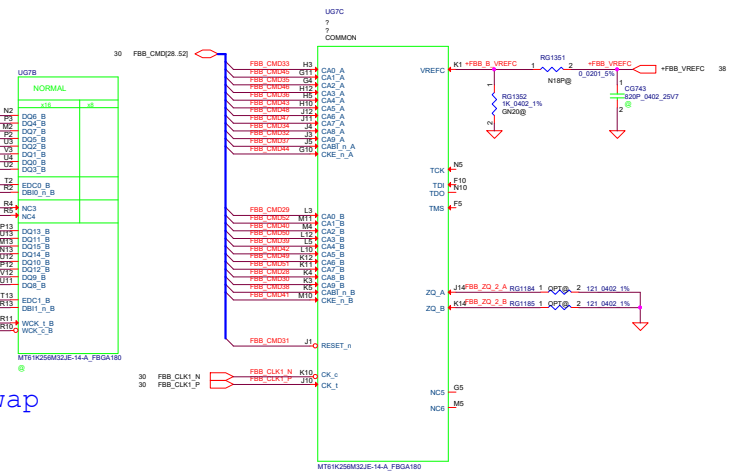




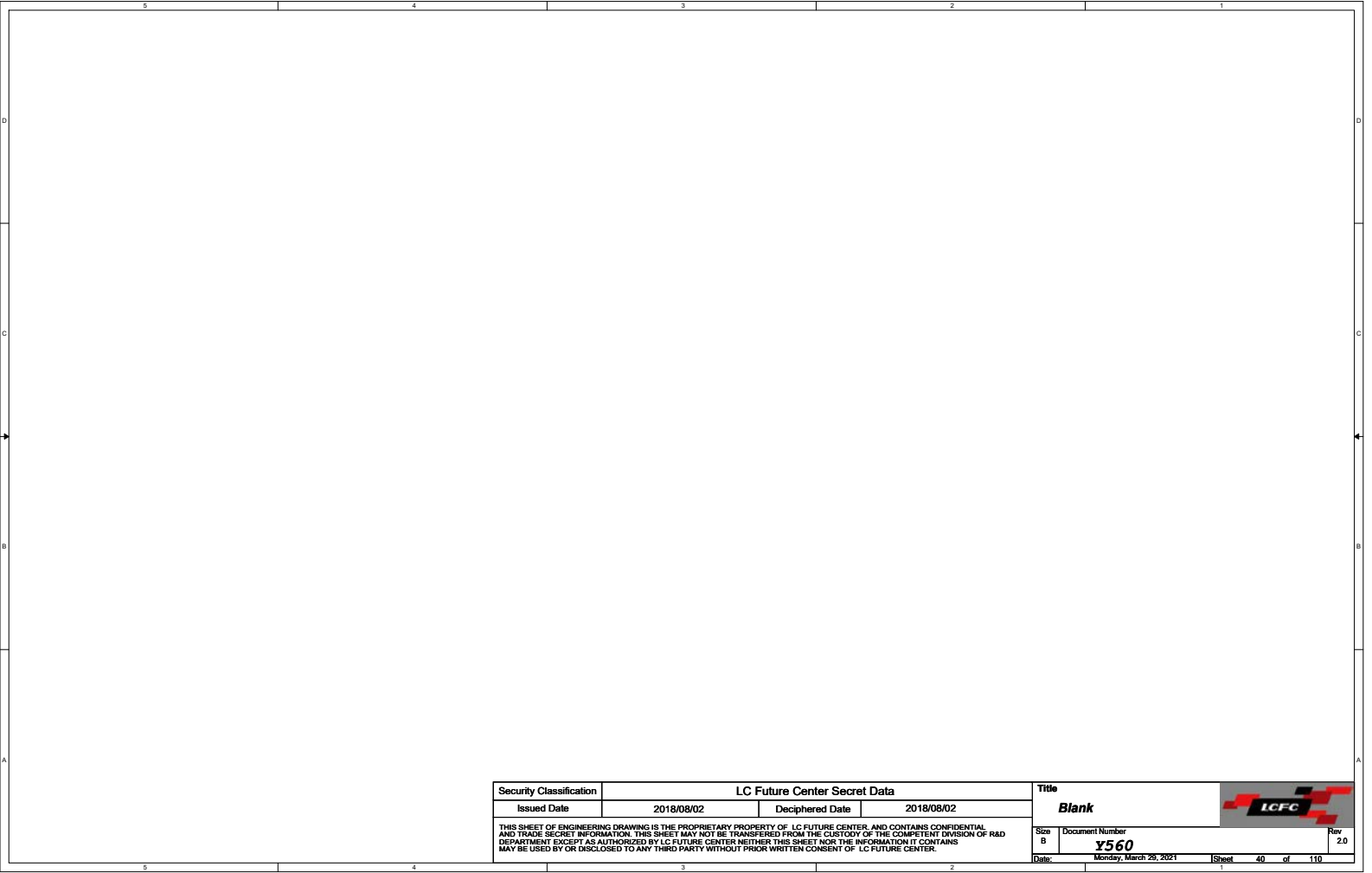
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Issued Date	2018/08/02	Deciphered Date	2018/08/02		
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				Date: <b>Monday, March 26, 2021</b>	Sheet <b>37</b> of <b>110</b>



VBREFC IS NOT USED IN  
x16 CONFIGURATION  
1K OHM PULL-DOWN IS  
IN PLACE OF THE 1.33K  
FOR RV1183



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Title		
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Size B	Document Number <b>Y560</b>	
Date	Monday, March 28, 2021	Rev 2.0
Sheet 40 of 110		

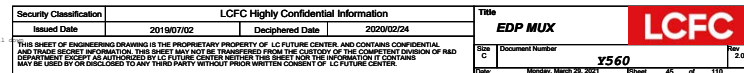








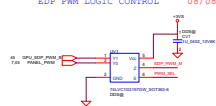




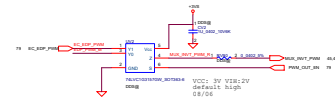


EDP PWM LOGIC CONTROL

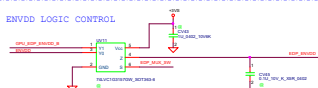
need fine tune RG107 RG108 RG88 BOM structure 08/08



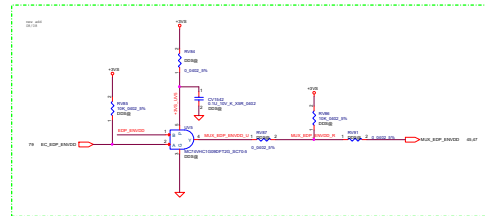
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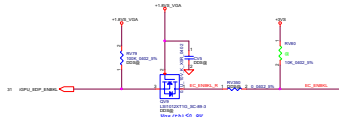
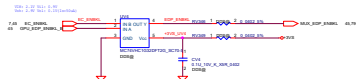
Co-Lay EDP ENVDD LOGIC CONTROL



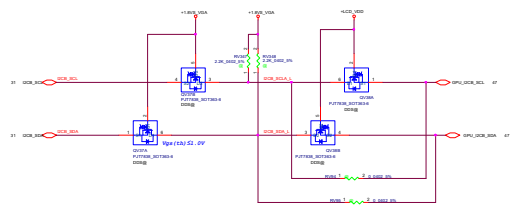
EDP ENVDD LOGIC CONTROL



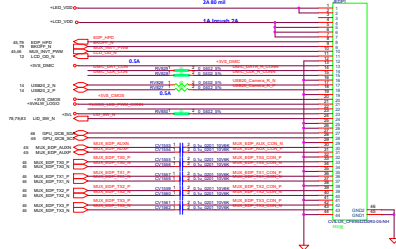
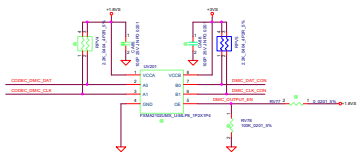
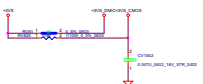
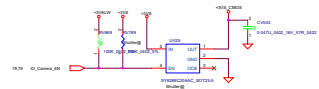
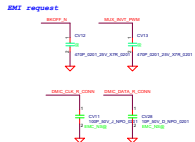
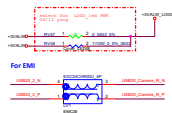
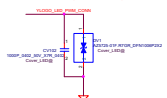
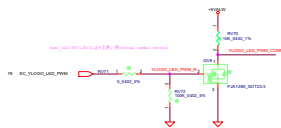
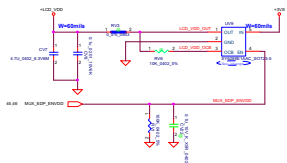
EDP backlight LOGIC CONTROL



level shift for I2C



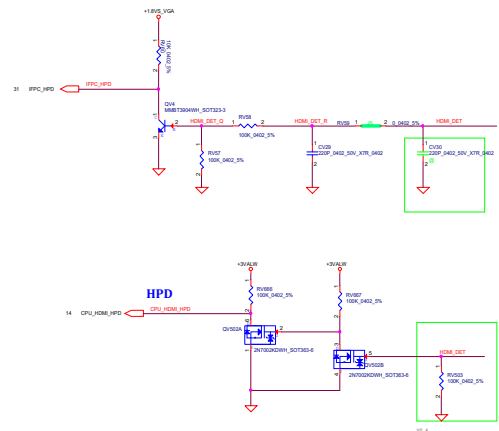
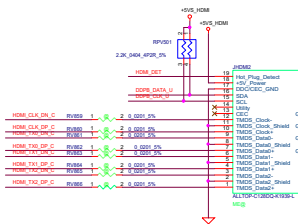
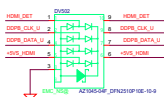
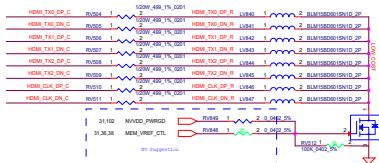
### LCD POWER CIRCUIT






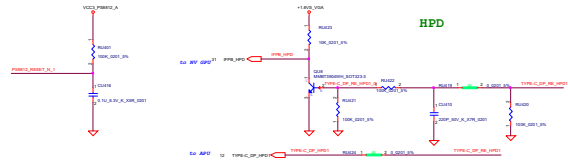
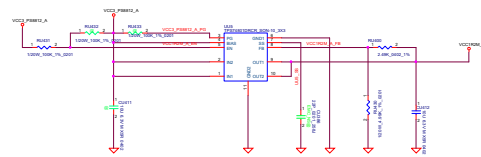
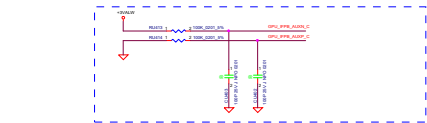
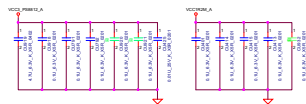


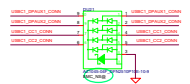
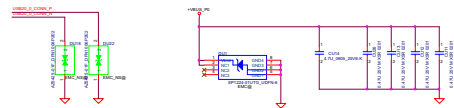
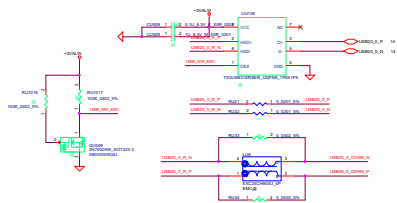
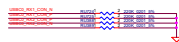
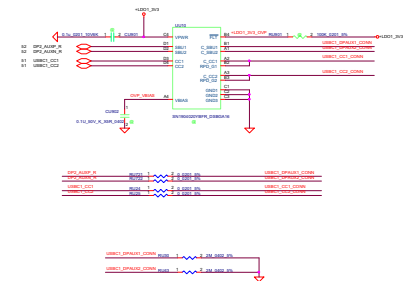


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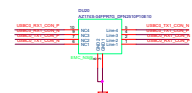
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Issued Date	2019/07/02	Declassified Date	2020/02/24			
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Doc Number	Y560		Doc	Document Number	Per 2	
Doc	Monday, March 26, 2021		Doc	30	of 110	

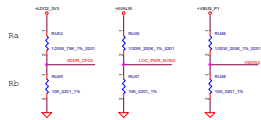




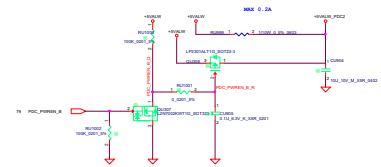
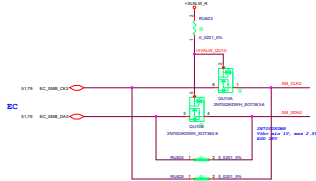
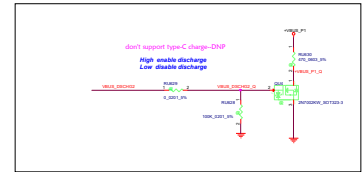
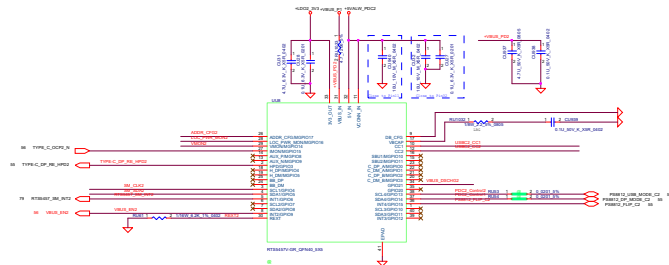


DU19 & DU20 Change to SC300007A00 用此料号做BOM

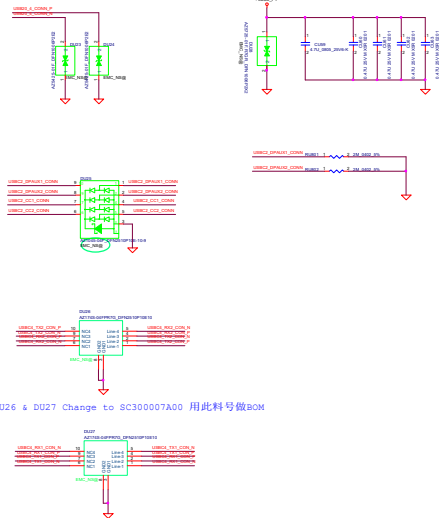
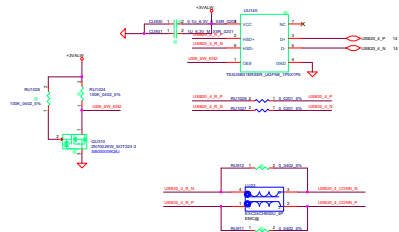
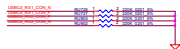
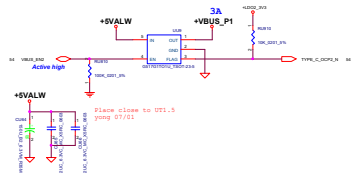




Slave Addr	Ra	Rb
addr0 : 0x00	10K	10K
addr1 : 0x01	10K	10K
addr2 : 0x02	10K	10K
addr3 : 0x03	10K	10K

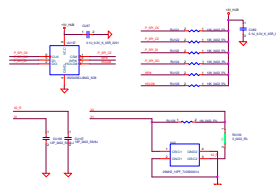
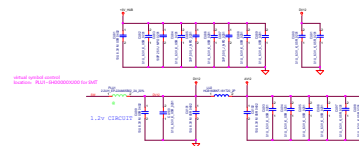
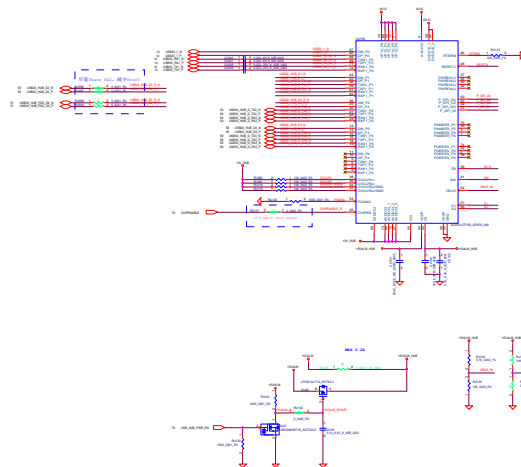
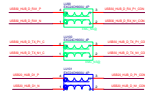
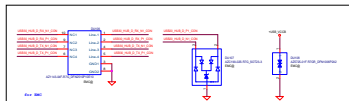
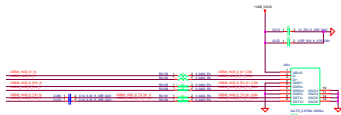




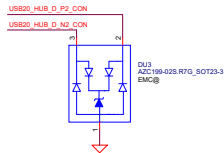
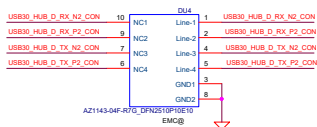
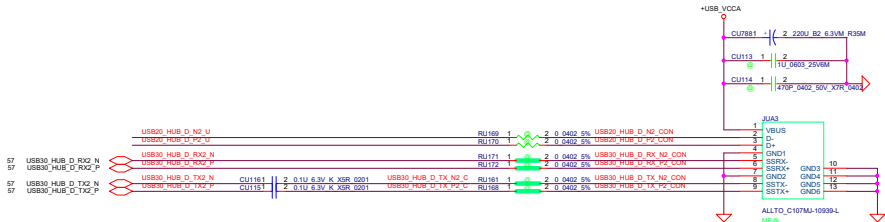


DU26 & DU27 Change to SC300007A00 用此料号做BOM

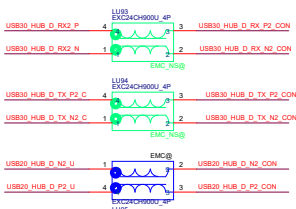






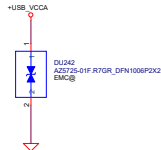


for EMC

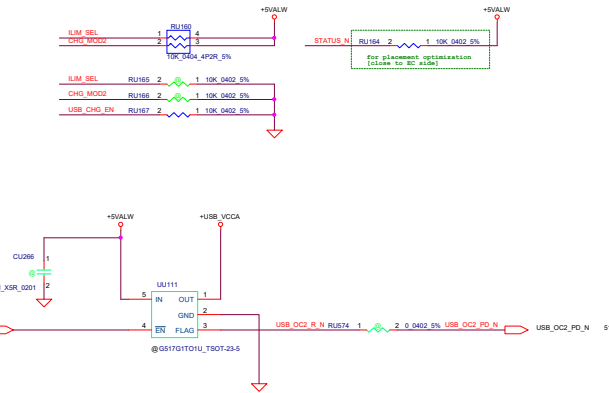
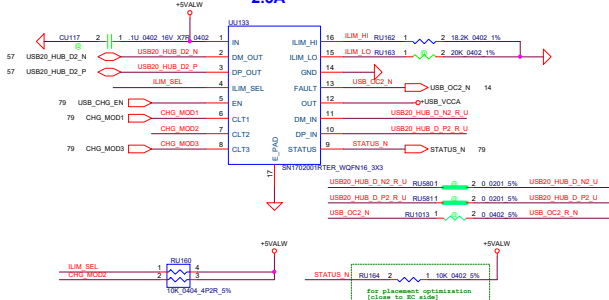


for EMC

10/16 david.mofy

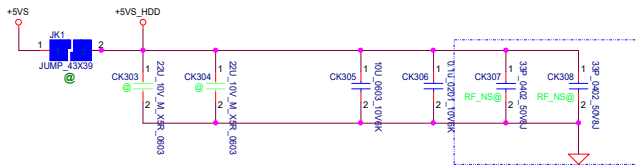


## USB charger 2.5A



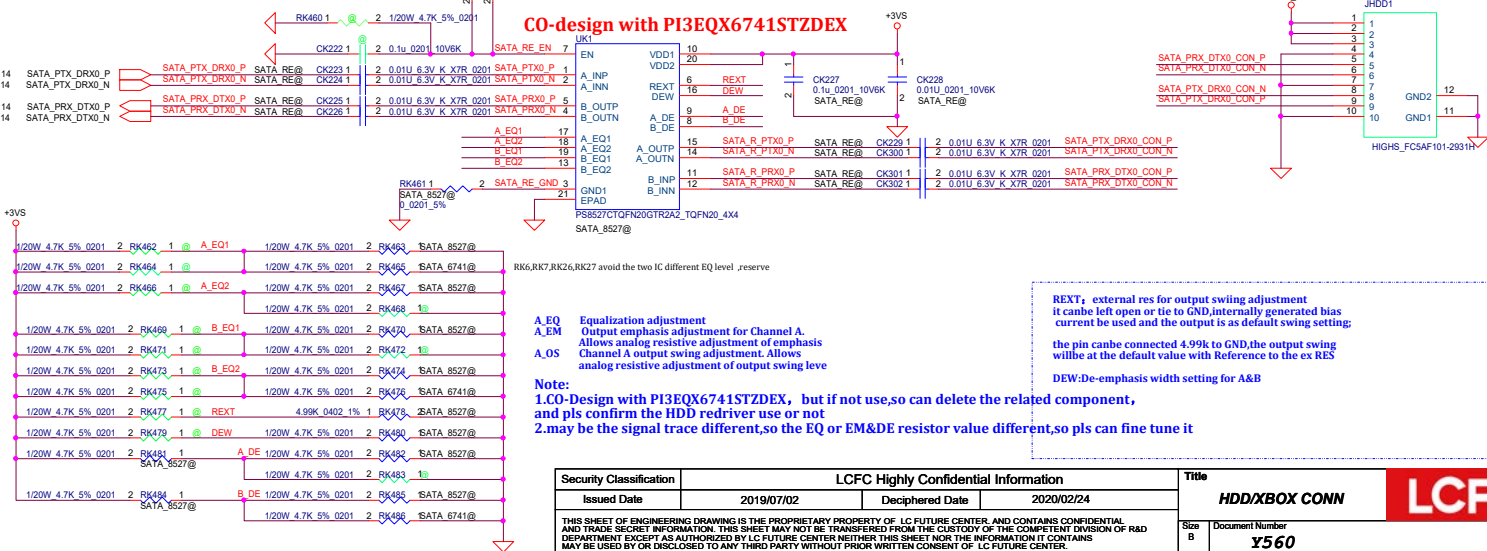
Delete USB2.0 HUB


### HDD Power



### HDD with Redriver Only For 17' Type

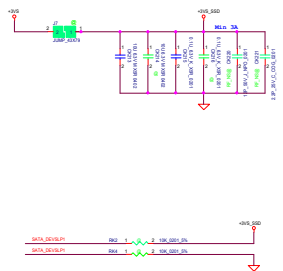
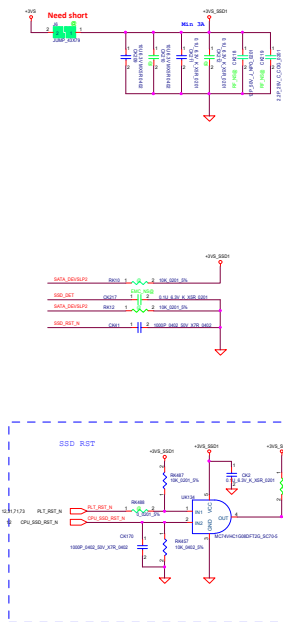
Add RK31 0627



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Issued Date		Deciphered Date		HDD/XBOX CONN		
2019/07/02		2020/02/24				
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Size		Document Number				Rev
		Y560				2.0
Date		Monday, March 26, 2021		Sheet		61 of 110

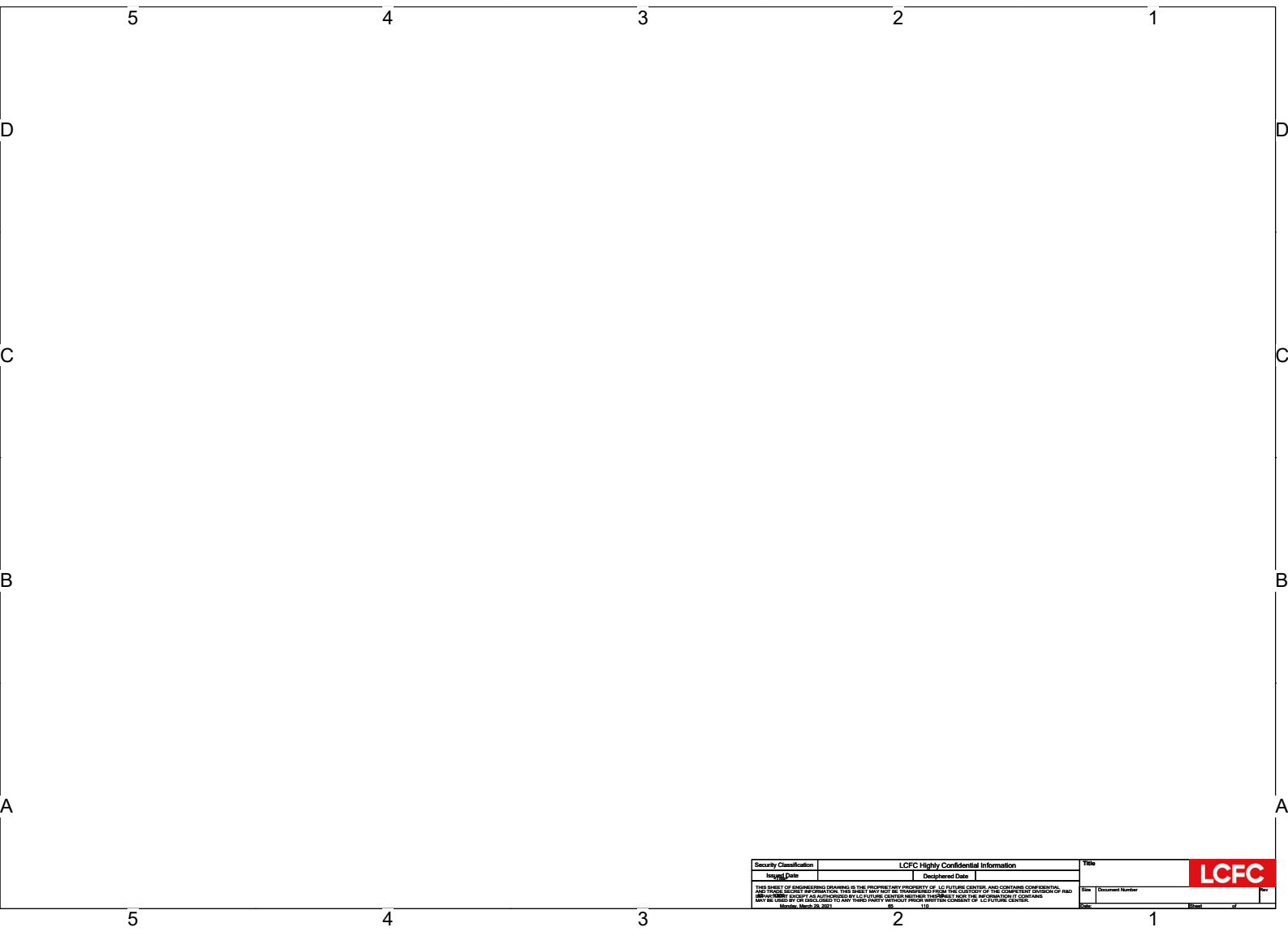


### *M.2 SSD0(PCIE)*

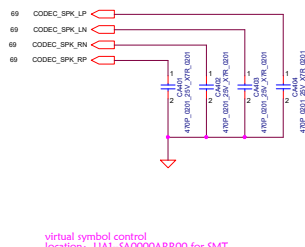
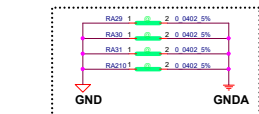
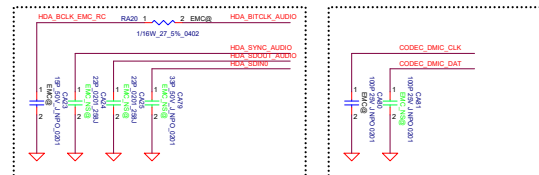
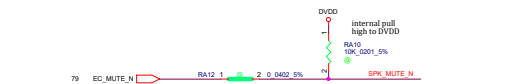
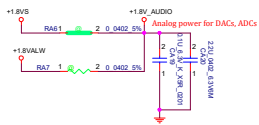
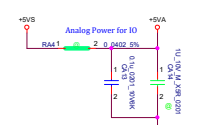
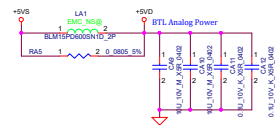
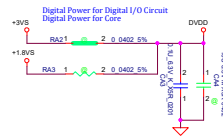


Delete USB3.0 Reapter Remove to DB board



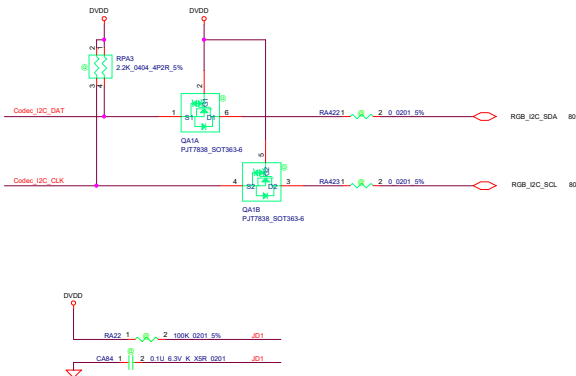
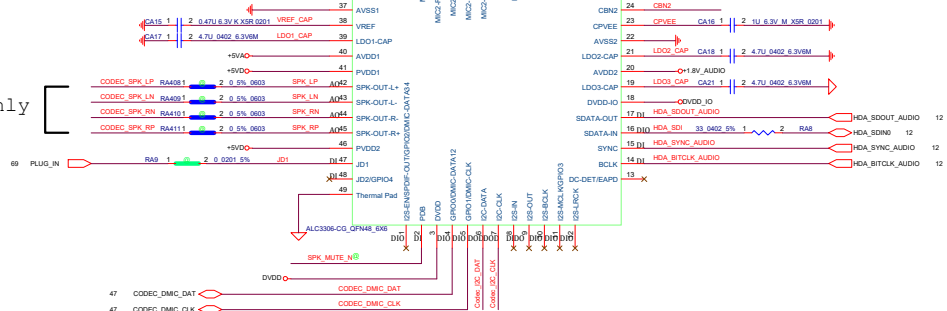


Security Classification		LCFC Highly Confidential Information		Title	
Issued Date		Declassified Date		LCFC	
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				Date	Sheet



virtual symbol control  
location: UA1--SA0000ARR00 for SMT

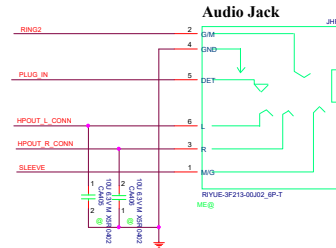
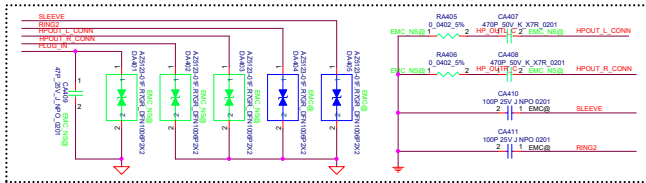
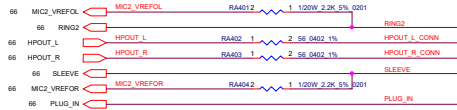
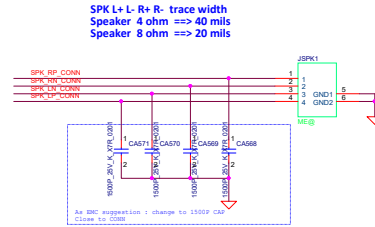
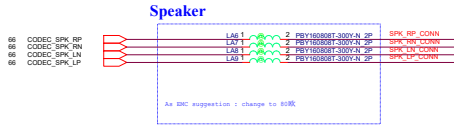
Vendor update MPN to ALC3306-VA1-CG  
New LCFC PN is SA0000ARR00  
Use vitural symbol untill new CIS symbol update



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					Y560
				Date	Monday, March 29, 2021
				Sheet	66 of 110

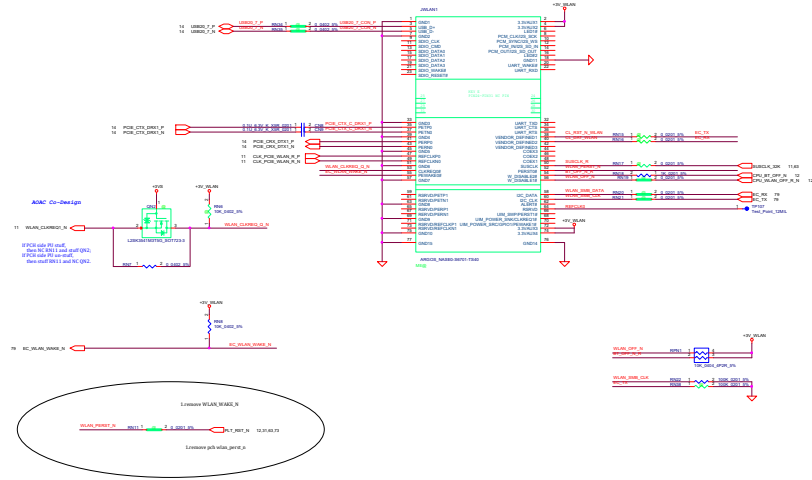
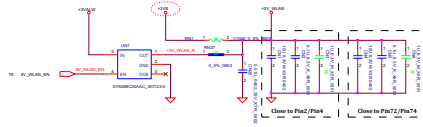






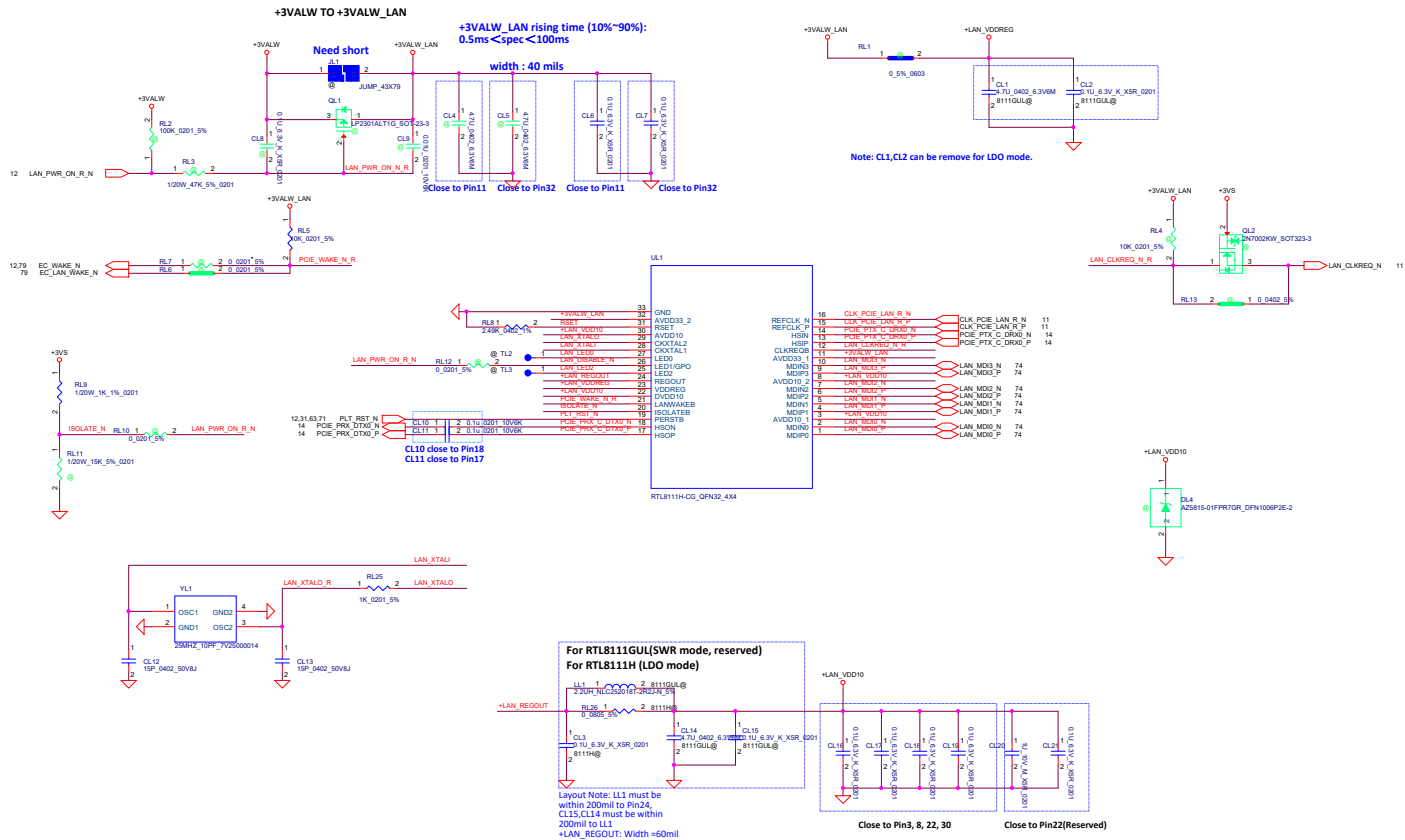


# Mini-Express Card(WLAN/WiMAX) Copy Wlan common design

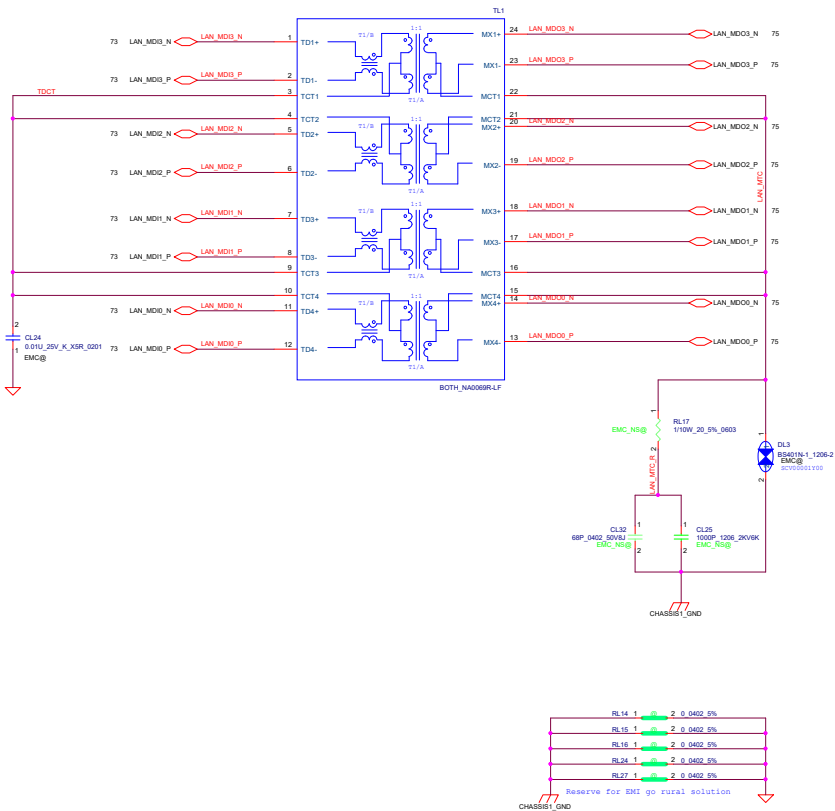
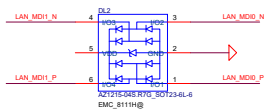
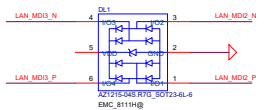




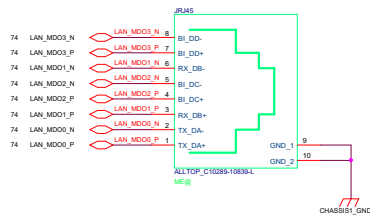




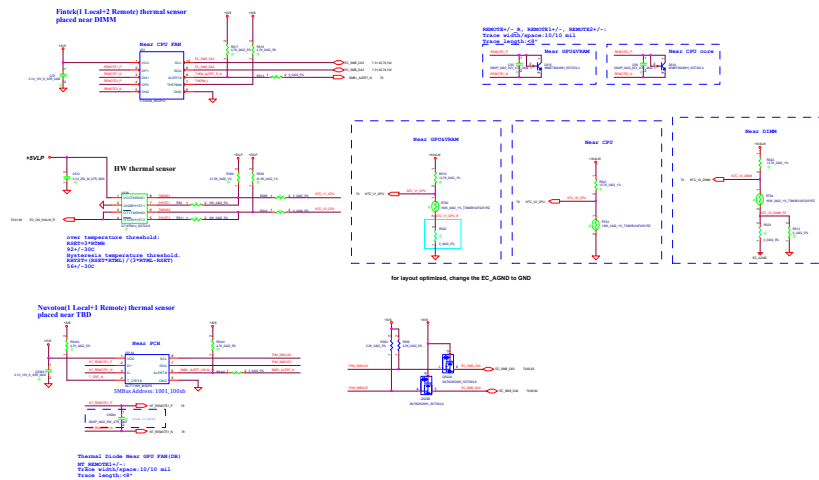
DL1/DL2  
1'S PN:SC300005900  
Place Close to TL1

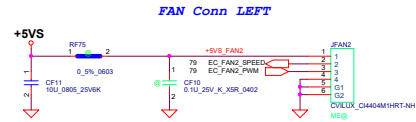
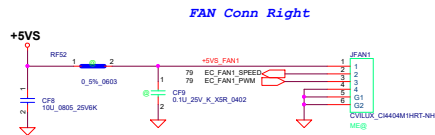


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				Sheet	74 of 110

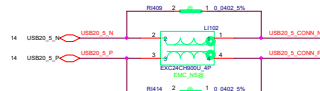


## Thermal Sensor



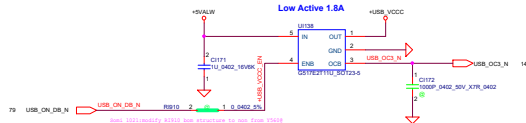


Right Side USB2.0 Port X 1 (USB/B)

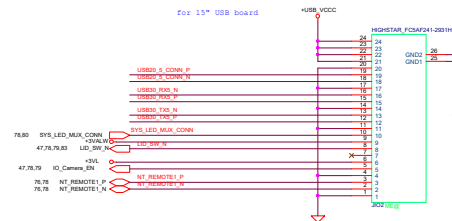


USB3.1 PORT x1

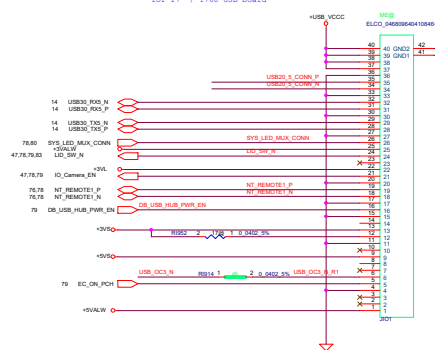
Low Active 1.8A

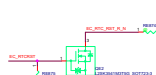
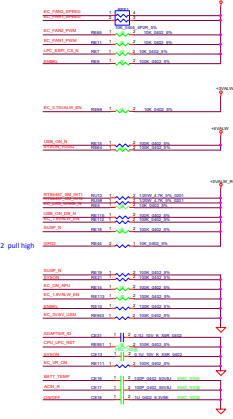
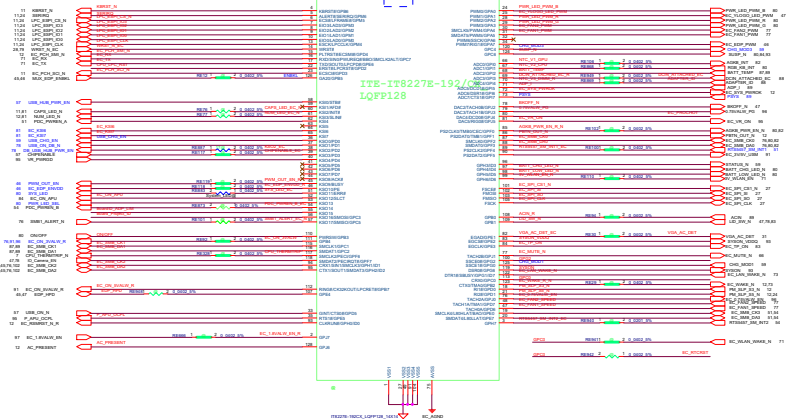
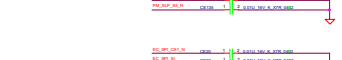
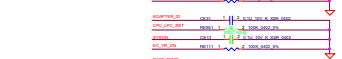
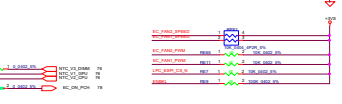
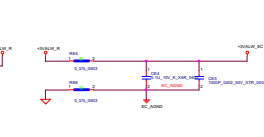
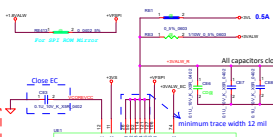
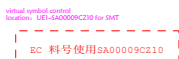
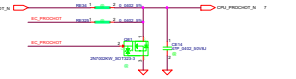
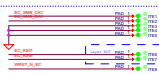
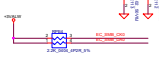
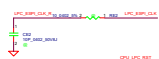


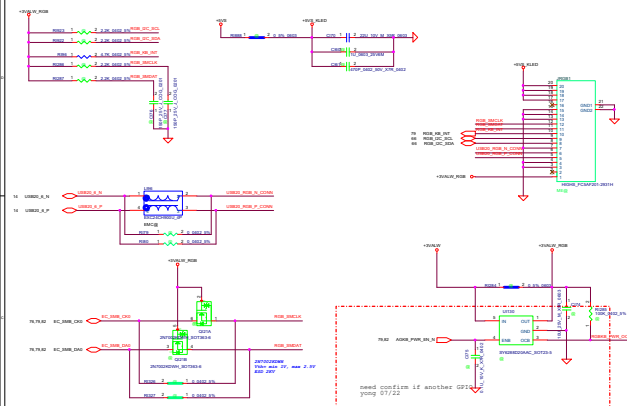
for 15" USB board



for 17" / Y760 USB board



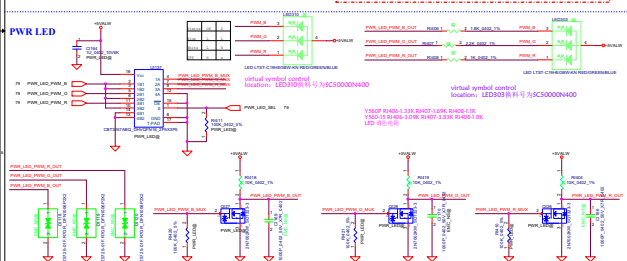




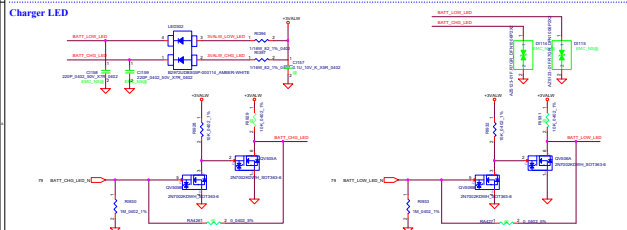
For Y760 KB lighting  
04/27 delete for P

For Y760 system lighting  
04/27 delete for P

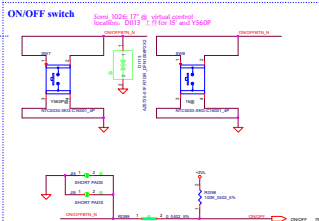
# PWR LED



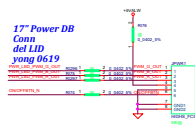
# Charger LED



# ON/OFF switch

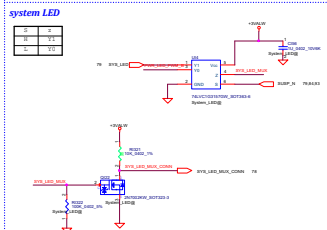


17" Power DB  
Conn  
del LID  
yong 0619

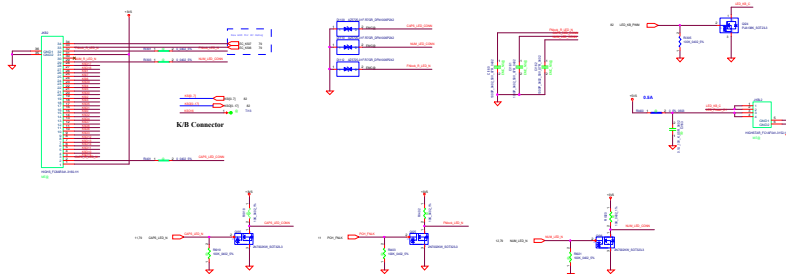


For P delete rear side ICON LED

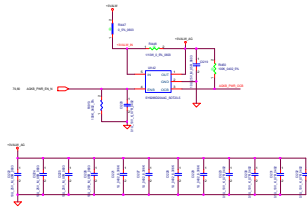
# system LED



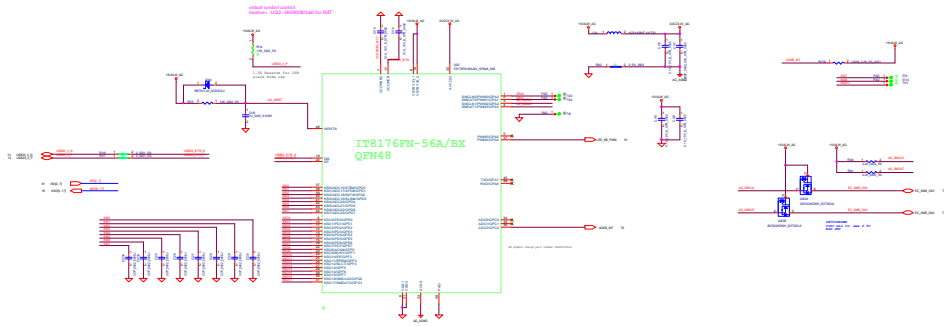


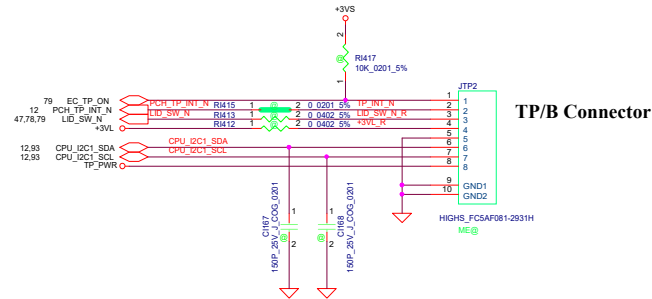
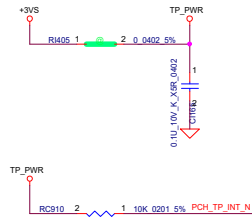
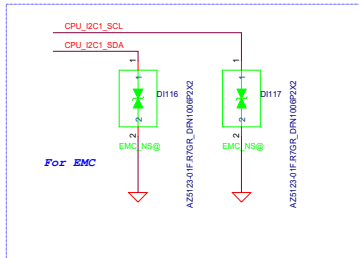


IT8258 delete for P

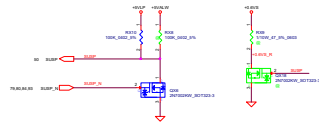


IT8176



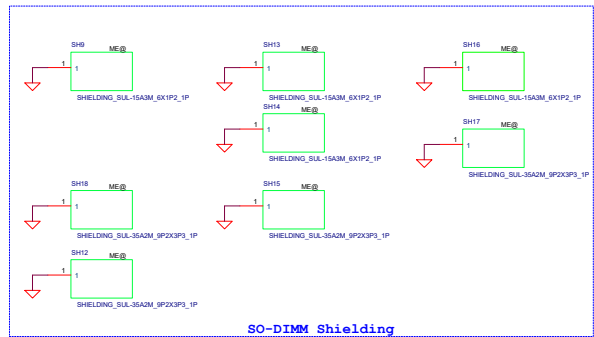
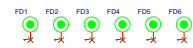
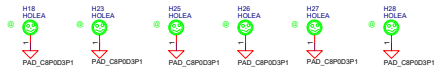
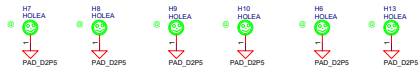


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Monday, March 29, 2021		83		110			
Date		Sheet		of		Rev	

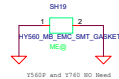
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B	Y560				2.0
Date:	Monday, March 28, 2021				Sheet 85 of 110



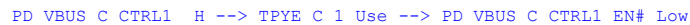
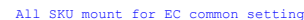


SO-DIMM Shielding



Y560 and Y760 SO Shield





Rev	0.1
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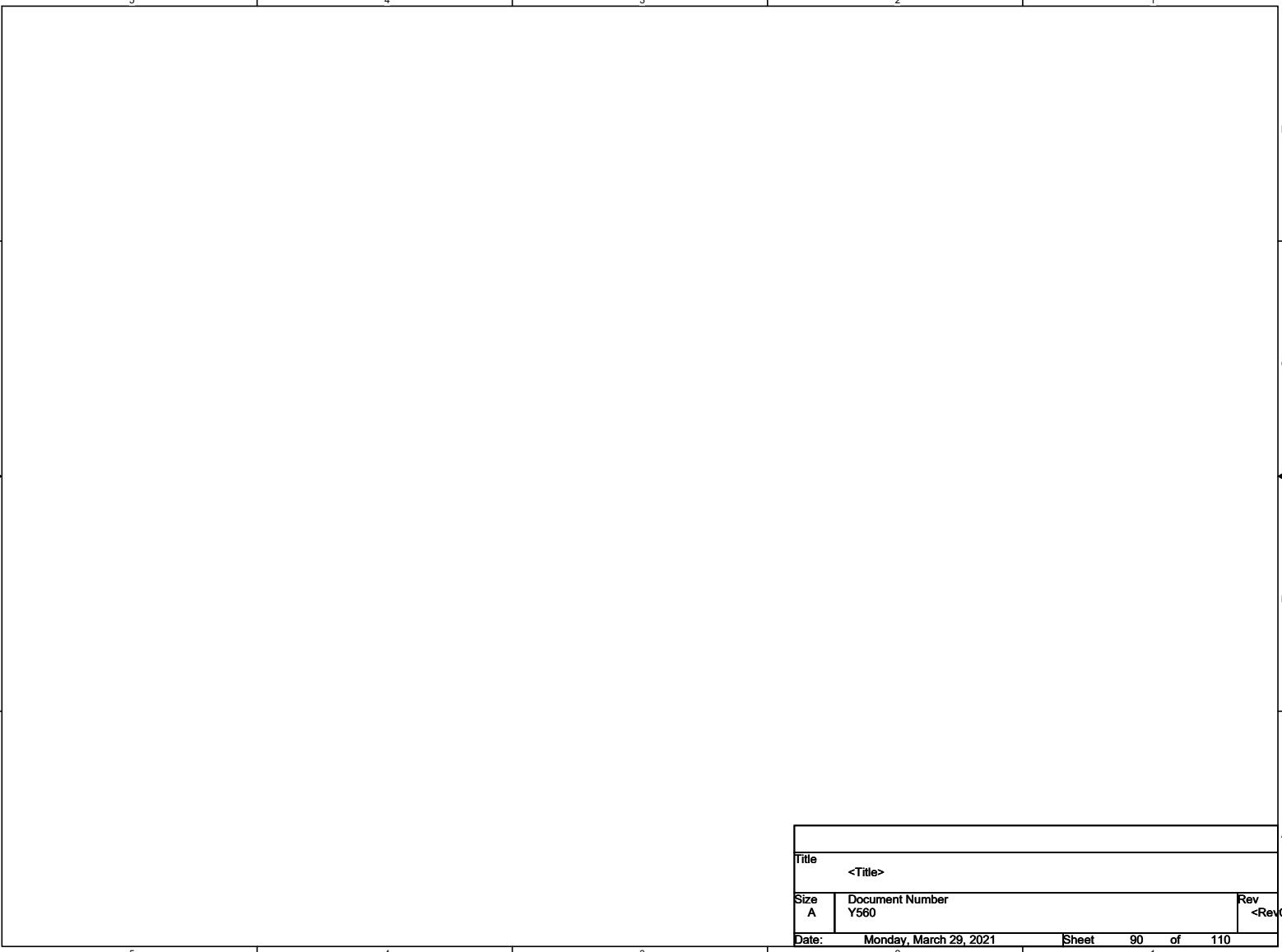


ACDET Threshold:min:1.787V  
BAT Max V=1.7,6V

PMON Gain=1uA/W Actual=0.5uA/W  
PR5415=15K 0.75V=100W

IchargeLM=16.1A  
IDischargeLM=64.4A

V charge (MAX):17.6V  
I charge (MAX):12A  
FSW:800K



5

4

3

2

1

D

D

C

C

B

B

A

A

Title			
<Title>			
Size	Document Number		Rev
A	Y560		<RevCo
Date:	Monday, March 29, 2021		Sheet 90 of 110

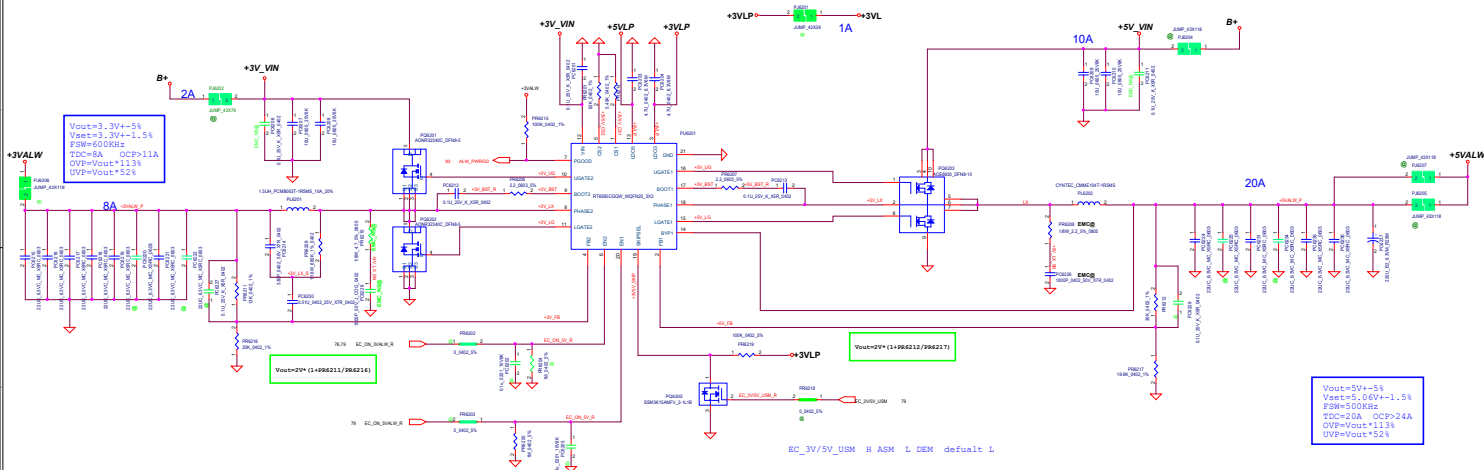
5

4

3

2

1



	RT6585C	RT6575D&TPS51275B
Mode	DEM/USM	USM/CCM
3V FSW	600K	355K
5V FSW	500K	300K
CSx	$R1\text{ limit} = (21\text{ limit} * R\text{dson}) * 8 / 50\mu$ $R2\text{ limit} = (21\text{ limit} * R\text{dson}) * 8 / 20\mu$	

RT6585B&TPS51285B BOM to BOM

RT6575D&TPS51275B BOM to BOM

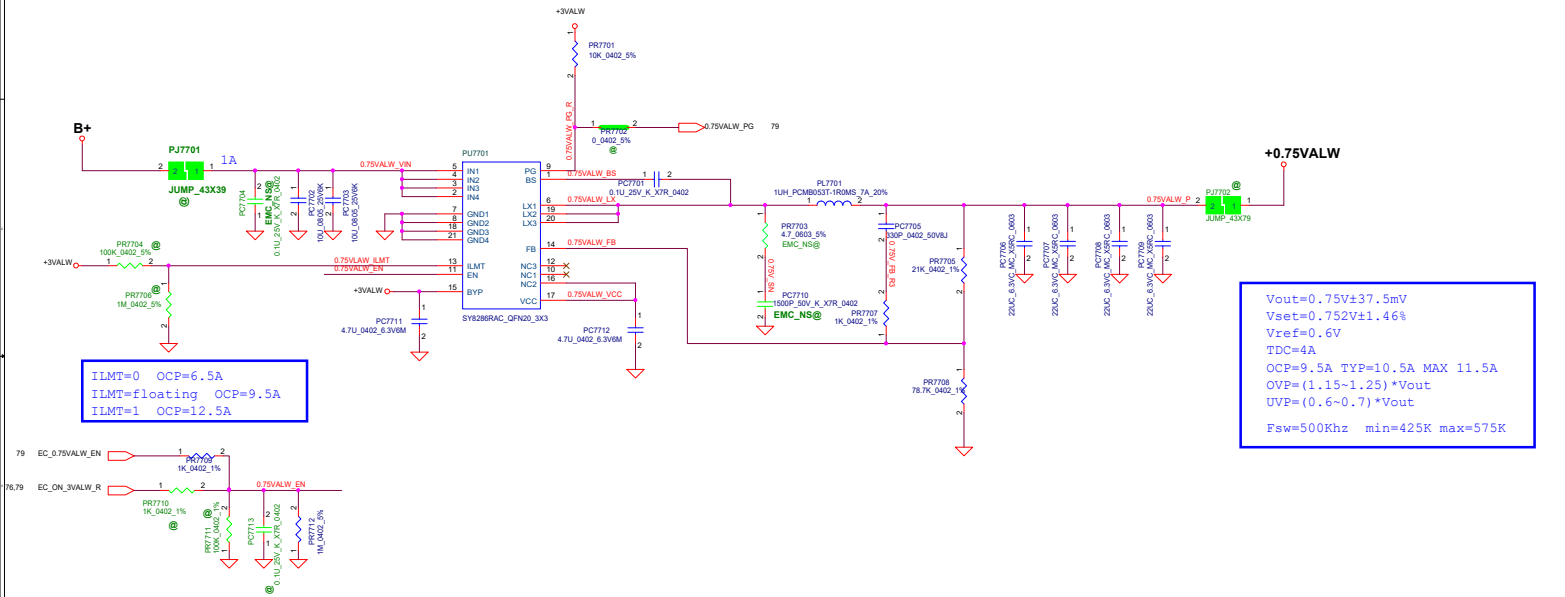
RT6585B&RT6575D PIN to PIN, with different work mode, FSW, and CS setting







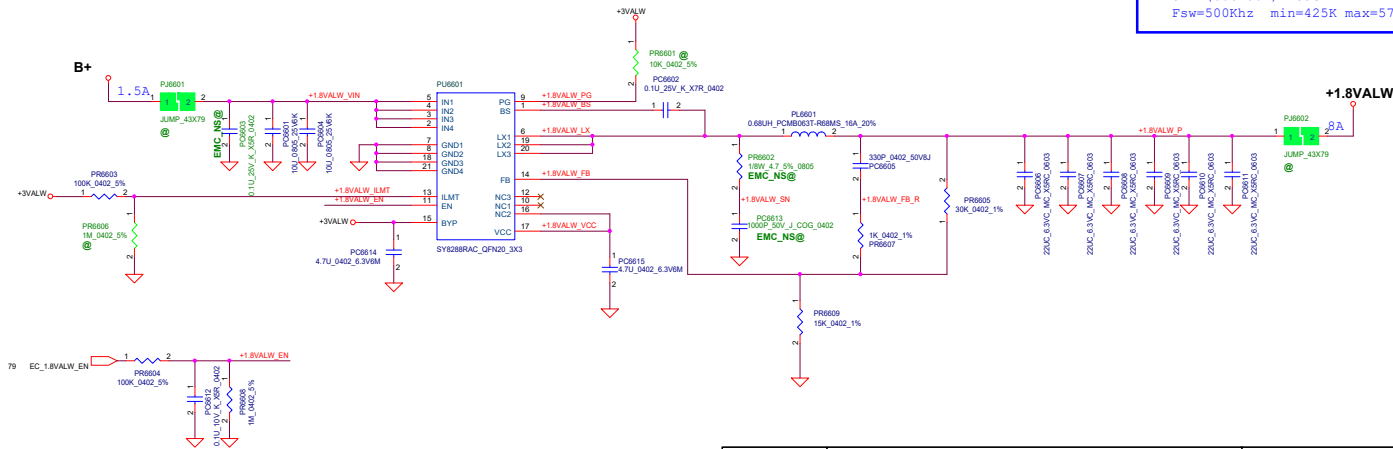




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Date:	Monday, March 26, 2021	Sheet	66	of	110



$V_{out}=1.8V\pm5\%$   
 $V_{set}=1.8V\pm2.3\%$   
 $V_{ref}=0.6V(+1\%)$   
 $TDC=8A$   
 $OCp=16A$   
 $OVp=(1.15\sim1.25)*V_{out}$   
 $UVp=(0.6\sim0.7)*V_{out}$   
 $F_{sw}=500Khz$  min=425K max=575K




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Date:	Monday, March 26, 2021		Sheet	97	of 110



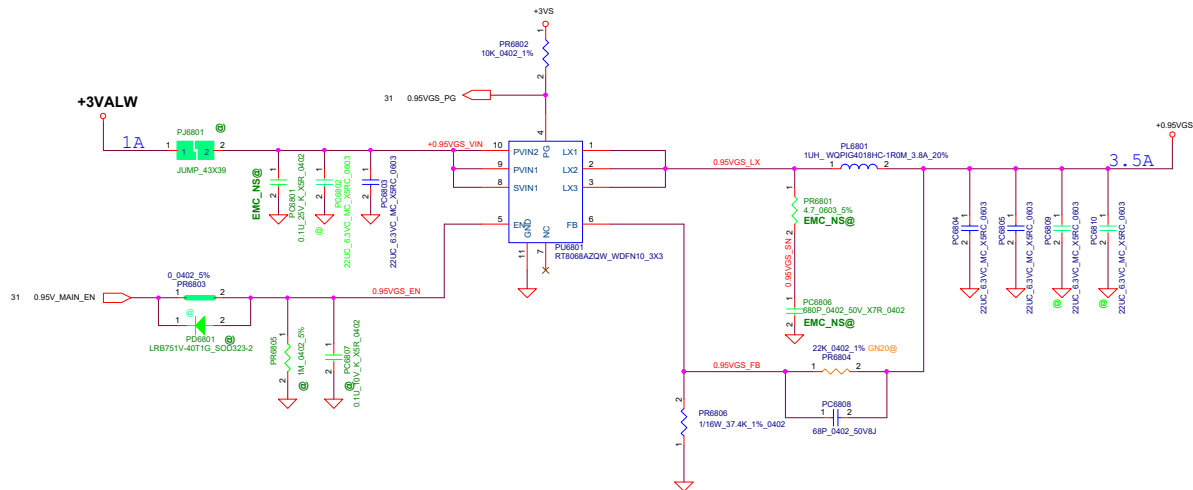
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Size	Document Number				Rev
C	Y560				0.1
Date	Monday, March 26, 2021		Sheet	88	of 118

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GN20 PR6804=22K  
 Vout=0.953V±3%  
 Vref=0.6V  
 OCP>4A  
 Fsw=1Mhz  
  
 N18P PR6804=26.1K  
 SD03426128J  
 Vout=0.953V±3%  
 Vref=0.6V  
 OCP>4A  
 Fsw=1Mhz

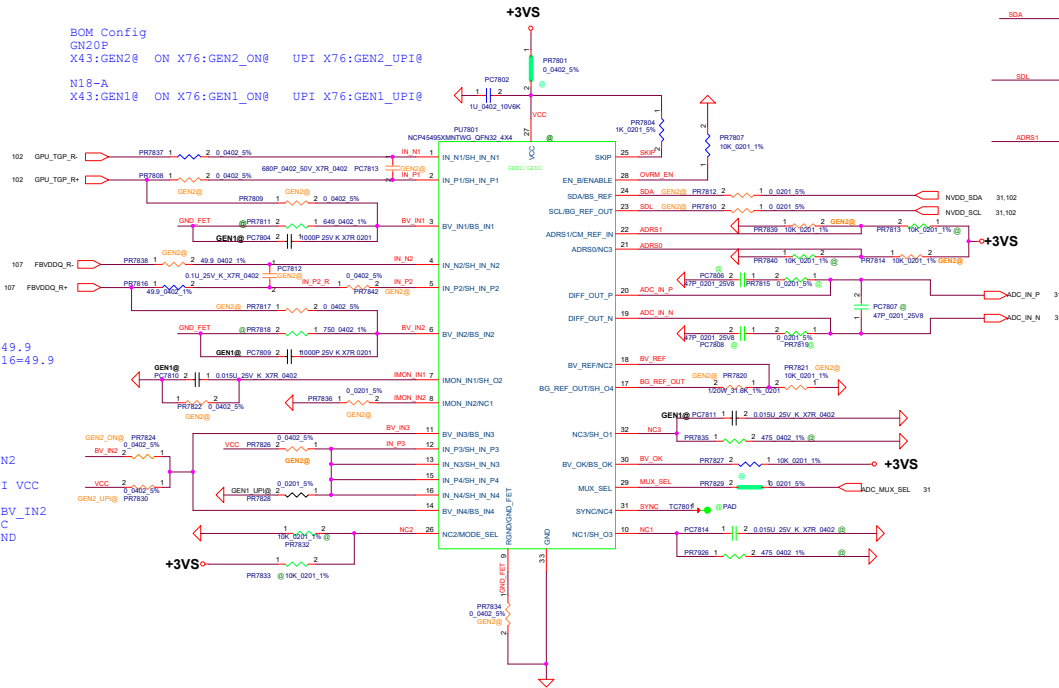
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR_GPU PWR			
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						Rev 0.1	
				Date:	Monday, March 29, 2021	Sheet	103 of 110




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				Date: Monday, March 29, 2021	Sheet 104 of 110	

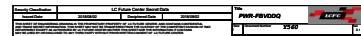


BCM Config  
 GN20P  
 X43:GEN2@ ON X76:GEN2\_ON@ UPI X76:GEN2\_UPI@  
 N18-A  
 X43:GEN1@ ON X76:GEN1\_ON@ UPI X76:GEN1\_UPI@




ADDR default is 0x6A(8 bit addr),  
 for 7bit addr is 0x35  
 a.ADDRS0(pin21): 10K PU 3.3v  
 b.ADDRS1(PIN 22): 10K PD to GND  
 00:0X34 01:0X35 10:0X36 11:0X37

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		GPU PWR Decoupling	
2018/08/02		2018/08/02			
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				Sheet 106 of 110	
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				Date Monday, March 26, 2024	Rev 0.1
				Sheet 110	of 110